PATENT
Attorney Docket No. 401572/Sakai

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
SHINYA SOEDA

Application No.	Unassigned	Art Unit:	Unassigned
Filed:	February 20, 2002	Examiner:	Unassigned
For:	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME		

REQUEST FOR APPROVAL OF DRAWING AMENDMENT

Commissioner for Patents
Washington, D. C. 20231

Dear Sir:

The Examiner is requested to approve the changes indicated in red on the attached copy of Figure 6A.

Respectfully submitted,

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Date: February 20, 2002
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PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D. C. 20231

Dear Sir:

Prior to the examination of the above-identified patent application, please enter the following amendments and consider the following remarks.

IN THE DRAWINGS:

The Examiner is requested to approve the changes to Figure 6A as indicated in the attached Request for Approval of Drawing Amendments.

IN THE SPECIFICATION:

Replace the paragraph beginning at page 1, line 4, with:

The present invention relates to a multilayer-circuit semiconductor device having resistors and signal line region(s) and a method of fabricating the same. Particularly, this invention relates to the semiconductor device preventing relative fluctuations in resistance among the resistors and, moreover, preventing fluctuations in interconnection capacitance (stray capacitance) because of the influence of the interconnection patterns in upper or lower layers of the signal-wiring, and to a method of fabricating this semiconductor device.

Replace the paragraph beginning at page 1, line 17, with:

Conventionally, data performed between LSI's, such as memories, microcomputers, and logic elements to control electrical equipment and to perform video and audio signal processing. However, eRAM (embedded RAM) obtained by integrating these LSI's into one chip, based on progress in both process and design technologies, has been intensively focused on as a new device (i.e., system LSI). The eRAM obtained by integrating ASIC's, microcomputers, and large-capacity memories can realize equipment that is more compact, has higher-speed data transfer due to expanded bus width, and has lower power consumption as compared to a combination of a general-purpose memory and a microcomputer.

Replace the paragraph beginning at page 2, line 4, with:

As semiconductor devices are becoming still more highly integrated, the structure of the semiconductor device is becoming more and more complicated. The number of layers of a multilayer-circuit for a logic system have increased. Because of such complicated structure, the disadvantages described below have occurred. Specifically, depending on whether an interconnection pattern is present on upper or lower layers of a layer on which resistors ("resistor group") or signal line region(s) are provided, there may occur problems, such as thermal influence over these groups and regions due to sintering

during fabrication of the semiconductor, influences caused by fluctuations in stray capacitance due to a difference of thicknesses of the layers, and electrical influence during operation of the semiconductor. Accordingly, it becomes more important whether the resistor group and the signal line region located in a logic region can be operated stably.

Replace the paragraph beginning at page 2, line 21, with:

Fig. 6A is a plan view of DRAM consolidated logic that has been conventionally used. This DRAM consolidated logic has a DRAM region E1 and a logic region E2. Fig. 13 and Fig. 14 show cross-sectional views taking along line XIII-XIII of Fig. 6A showing a structure covering a first Al interconnection layer of the DRAM consolidated logic in Fig. 6A. In this type of DRAM-logic hybrid device, a cylindrical stacked capacitor (concave) having a certain height is formed in the DRAM region E1. The stacked capacitor is composed of a lower capacitor electrode layer 122, dielectric film 123, and an upper capacitor electrode layer 124.

Replace the paragraph beginning at page 3, line 7, with:

Fig. 13 shows an example of the DRAM consolidated logic including a region having the resistor group composed of a group of diffused resistors in the logic region E2. The resistor group arranged in the logic region E2 is provided to be used as additional resistors. In Fig. 13, the resistor group is composed of the belt-like isolation oxide films 105 spaced apart from and extending in parallel with each other on the main surface of the semiconductor substrate, and N^+ diffused regions 104 each extending between the belt-like isolation oxide films 105. The first Al interconnection layer 129 is located on the upper layer of the resistor group in the logic region E2.

Replace the paragraph beginning at page 3, line 19, with:

Fig. 14 shows an example of the DRAM consolidated logic including a region having the signal interconnection in the logic region E2. In Fig. 14, two different layers of signal interconnections are located in the logic region E2, that is, a signal interconnection 126a formed by utilizing a layer common to a bit line 126 in the DRAM region E1, and a signal interconnection 108a formed by utilizing a layer common to a gate electrode in the DRAM region E1. The first Al interconnection layer 129 is located above the region having the signal interconnections 108a and 126a.

Replace the paragraph beginning at page 4, line 4, with:

In the conventional art, however, in association with an increase in the number of interconnection layers in the logic region E2, the resistor group and the signal interconnection in the logic region E2 are affected by how a pattern is arranged on the upper layer or the lower layer. Therefore, the problems as follows occur.

Replace the paragraph beginning at page 4, line 10, with:

Firstly, there is a problem that relative resistance within the resistor group fluctuates depending on whether a pattern is present on the first Al interconnection layer 129 as the upper layer. For example, when any faults on a substrate produced due to etching or the like during fabrication are to be removed by sintering executed after formation of the first Al interconnection, removal of the faults on the substrate may become non-uniform due to presence or absence of a pattern on the first Al interconnection layer 129 as the upper layer. Traps caused by a boundary potential on the surface of the resistors may become non-uniform within the resistor group. Therefore, fluctuations in the relative resistance within the resistor group in an analog line or the like become a problem (see Fig. 13)

Replace the paragraph beginning at page 4, line 25, with:

Secondly, by patterning the signal interconnections 108a and 126a under the first Al interconnection layer 129, a difference in an interlayer thickness under the first Al interconnection layer 129 occurs between a portion having a signal pattern and a portion not having a signal pattern, stray capacitance to the base fluctuates, and a difference occurs between actual resistance and the simulated resistance during circuit design (see Fig. 14). The fluctuation in stray capacitance becomes a serious problem in the pattern in which a change of the signal interconnection or the like is not desirable. Further, during operation of the semiconductor device, the signal interconnection is electrically affected by the pattern of other signal interconnection on the upper layer or the lower layer. Therefore, stable signal circuit cannot be obtained.

IN THE CLAIMS

Replace the indicated claims with:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate having a plurality of regions;

a resistor group including a plurality of resistors located in one of said regions of said semiconductor substrate;

a metal interconnection layer opposite the region in which said resistor group is located; and

a shielding layer between said resistor group and said metal interconnection layer.

2. (Amended) The semiconductor device according to claim 1, comprising at least one DRAM region and one logic region, including a layer common to a bit line layer in said DRAM region and used as said shielding layer in said logic region.

3. (Amended) The semiconductor device according to claim 1, comprising

at least one DRAM region with a stacked capacitor and one logic region, wherein said stacked capacitor in said DRAM region includes a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, and

a layer common to said upper capacitor electrode layer in said DRAM region and used as said shielding layer in said logic region.

4. (Amended) The semiconductor device according to claim 1, wherein said shielding layer has a fixed potential.

5. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a signal interconnection layer on said semiconductor substrate; and

a shielding layer on at least one side of said signal interconnection layer.

6. (Amended) The semiconductor device according to claim 5, comprising at least one DRAM region and one logic region, including a layer common to a gate electrode layer in said DRAM region and used as said shielding layer in said logic region.

7. (Amended) The semiconductor device according to claim 5, comprising at least one DRAM region and one logic region, including a layer common to a bit line layer in said DRAM region and used as said shielding layer in said logic region.

8. (Amended) The semiconductor device according to claim 5, comprising

at least one DRAM region with a stacked capacitor and one logic region, wherein said stacked capacitor in said DRAM region includes a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, and

a layer common to said upper capacitor electrode layer in said DRAM region and used as said shielding layer in said logic region.

9. (Amended) The semiconductor device according to claim 5, wherein said shielding layer has a fixed potential.

10. (Amended) A method of fabricating a semiconductor device having at least one DRAM region and one logic region and having a resistor group in said logic region, the method comprising:

forming a resistor group in said logic region;

forming a shielding layer in said DRAM region and said logic region; and

forming a metal interconnection layer opposite a portion of said logic region where said resistor group is located.

12. (Amended) The method according to claim 10, further comprising forming a stacked capacitor having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said capacitor electrode layer is said shielding layer.

13. (Amended) The method according to claim 10, further comprising fixing potential of said shielding layer.

14. (Amended) A method of fabricating a semiconductor device having at least one DRAM region and one logic region and having a signal interconnection layer in said logic region, the method comprising:

forming a signal interconnection layer in said logic region; and

forming a shielding layer on at least one side of said signal interconnection layer in said DRAM region and said logic region.

17. (Amended) The method according to claim 14, further comprising forming a stacked capacitor having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said capacitor electrode layer is said shielding layer.

18. (Amended) The method according to claim 14, further comprising fixing potential of said shielding layer.

IN THE ABSTRACT

Replace the abstract with:

ABSTRACT OF THE DISCLOSURE

A semiconductor device has a semiconductor substrate and a resistor group and/or a signal interconnection layer in a region of the semiconductor substrate. A shielding layer is located above and/or below the region where the resistor group and/or the signal interconnection layer are located.

REMARKS

The foregoing amendments are made to correct minor translational errors and to meet United States requirements as to form. No new matter is added.

Respectfully submitted,

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AMENDMENTS TO SPECIFICATION, CLAIMS, AND ABSTRACT MADE VIA PRELIMINARY AMENDMENT

Amendments to the paragraph beginning at page 1, line 4:

The present invention relates to a multilayer-circuit ~~type~~ semiconductor device having resistors and signal line region(s) and a method of fabricating the same. Particularly, this invention relates to the semiconductor device ~~capable of~~ preventing relative fluctuations in resistance among the resistors and, moreover, preventing fluctuations in interconnection capacitance (stray capacitance) because of the influence of the interconnection patterns in upper or lower layers of the signal-wiring, and to ~~the~~ a method of fabricating this semiconductor device.

Amendments to the paragraph beginning at page 1, line 17:

Conventionally, data ~~transaction is~~ transactions are performed between LSI's, such as memories, microcomputers, and ~~logics~~ logic elements to control ~~an~~ electrical equipment and to perform video and audio signal processing. However, eRAM (embedded RAM) obtained by integrating these LSI's into one chip, based on progress in both process and design technologies, has been intensively focused on as a new device

(i.e., system LSI). The eRAM obtained by integrating ASIC's, microcomputers, and large-capacity memories can realize ~~the~~ equipment that is more compact, has higher-speed data transfer due to expanded bus width, and has lower power consumption as compared to a combination of a general-purpose memory and a microcomputer.

Amendments to the paragraph beginning at page 2, line 4:

As ~~the~~ semiconductor ~~device is micromachined more and~~ devices are becoming still more highly integrated, the structure of the semiconductor device is becoming more and more complicated. ~~Number~~The number of layers of a multilayer-circuit for a logic system have increased. Because of such complicated structure, the disadvantages described below have occurred. Specifically, depending on whether an interconnection pattern is present on upper or lower layers of a layer on which resistors ("resistor group") or signal line region(s) are provided, there may occur ~~the~~ problems, such as thermal influence over these ~~group~~ groups and ~~region~~ regions due to sintering during fabrication of the semiconductor, ~~influence~~ influences caused by fluctuations in stray capacitance due to a difference of ~~film thickness between~~ thicknesses of the layers, and electrical influence during operation of the semiconductor. Accordingly, it becomes more important whether the resistor group and the signal line region ~~provided~~ located in a logic region can be operated stably.

Amendments to the paragraph beginning at page 2, line 21:

Fig. 6A is a plan view of DRAM consolidated logic that has been conventionally used. This DRAM consolidated logic has a DRAM region E1 and a logic region E2. Fig. 13 and Fig. 14 show cross-sectional views taking along ~~lines A-A'~~ line XIII-XIII of Fig. 6A showing a structure covering a first Al interconnection layer of the DRAM consolidated logic in Fig. 6A. In this type of DRAM-logic hybrid device, a cylindrical stacked capacitor (concave) having a certain height is formed in the DRAM region E1. The stacked capacitor is composed of a lower capacitor electrode layer 122, dielectric film 123, and an upper capacitor electrode layer 124.

Amendments to the paragraph beginning at page 3, line 7:

Fig. 13 shows an example of the DRAM consolidated logic including a region having the resistor group composed of a group of diffused resistors in the logic region E2. The resistor group arranged in the logic region E2 is ~~formed~~ provided to be used as additional resistors. In Fig. 13, the resistor group is composed of the belt-like isolation oxide films 105 spaced apart from and extending in parallel with each other on the main surface of the semiconductor substrate, and N^+ diffused regions 104 each extending between the belt-like isolation oxide films 105. The first Al interconnection layer 129 is ~~formed~~ located on the upper layer of the resistor group in the logic region E2.

Amendments to the paragraph beginning at page 3, line 19:

Fig. 14 shows an example of the DRAM consolidated logic including a region having the signal interconnection in the logic region E2. In Fig. 14, two different layers of signal ~~interconnection~~ interconnections are ~~formed~~ located in the logic region E2, that is, a signal interconnection 126a formed by utilizing a layer common to a bit line 126 in the DRAM region E1, and a signal interconnection 108a formed by utilizing a layer common to a gate electrode in the DRAM region E1. The first Al interconnection layer 129 is ~~formed~~ located above the region having the signal interconnections 108a and 126a.

Amendments to the paragraph beginning at page 4, line 4:

In the conventional art, however, in association with an increase in the number of interconnection layers in the logic region E2, the resistor group and the signal interconnection ~~formed~~ in the logic region E2 are affected by how a pattern is arranged on the upper layer or the lower layer. Therefore, the problems as follows occur.

Amendments to the paragraph beginning at page 4, line 10:

Firstly, there is a problem that relative resistance within the resistor group fluctuates depending on whether a pattern is present on the first Al interconnection layer 129 as the upper layer. For example, when any faults on a substrate produced due to etching or the like during fabrication are to be ~~recovered~~ removed by sintering executed after formation of the first Al interconnection, ~~recovery~~ removal of the faults on the substrate may become non-uniform due to presence or absence of a pattern on the first Al interconnection layer 129 as the upper layer. Traps caused by a boundary potential on the surface of the resistors may become non-uniform within the resistor group. Therefore, fluctuations in the relative resistance within the resistor group in an analog line or the like become a problem (see Fig. 13)

Amendments to the paragraph beginning at page 4, line 25:

Secondly, by patterning the signal interconnections 108a and 126a under the first Al interconnection layer 129, a difference in an interlayer ~~film~~ thickness under the first Al interconnection layer 129 occurs between a portion having a signal pattern and a portion not having a signal pattern, stray capacitance to the base fluctuates, and a difference occurs between actual resistance and the simulated ~~one~~ resistance during circuit design (see Fig. 14). The fluctuation in stray capacitance becomes a serious problem in the pattern in which a change of the signal interconnection or the like is not desirable. Further, during operation of the semiconductor device, the signal interconnection is electrically affected by the pattern of other signal interconnection ~~formed~~ on the upper layer or the lower layer. Therefore, stable signal circuit cannot be obtained.

Amendments to the existing claims:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate having a plurality of regions;

a resistor group including a plurality of resistors ~~provided~~ located in one of said regions of said semiconductor substrate;

a metal interconnection layer ~~above~~ opposite the region in which said resistor group ~~has been provided~~ is located; and

a shielding layer between said resistor group and said metal interconnection layer.

2. (Amended) The semiconductor device according to claim 1, comprising at least ~~a~~ one DRAM region and ~~a~~ one logic region, ~~wherein~~ including a layer common to a bit line layer in said DRAM region ~~is~~ and used as ~~a~~ said shielding layer in said logic region.

3. (Amended) The semiconductor device according to claim 1, comprising

at least ~~a~~ one DRAM region with a stacked capacitor and ~~a~~ one logic region, wherein said stacked capacitor in said DRAM region ~~is composed of~~ includes a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, and

a layer common to said upper capacitor electrode layer in said DRAM region ~~is~~ and used as ~~a~~ said shielding layer in said logic region.

4. (Amended) The semiconductor device according to claim 1, wherein ~~a potential of~~ said shielding layer ~~is~~ has a fixed potential.

5. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a signal interconnection layer on said semiconductor substrate; and

a shielding layer on at least one side of said signal interconnection layer ~~, or shielding layers on both sides of said signal interconnection layer~~.

6. (Amended) The semiconductor device according to claim 5, comprising at least ~~a~~ one DRAM region and ~~a~~ one logic region, ~~wherein~~ including a layer common to a gate electrode layer in said DRAM region ~~is~~ and used as ~~a~~ said shielding layer in said logic region.

7. (Amended) The semiconductor device according to claim 5, comprising at least ~~a~~ one DRAM region and ~~a~~ one logic region, ~~wherein~~ including a layer common to a bit line layer in said DRAM region ~~is~~ and used as ~~a~~ said shielding layer in said logic region.

8. (Amended) The semiconductor device according to claim 5, comprising

at least ~~a~~ one DRAM region with a stacked capacitor and ~~a~~ one logic region, wherein said stacked capacitor in said DRAM region ~~is composed of~~ includes a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, and

a layer common to said upper capacitor electrode layer in said DRAM region ~~is~~ and used as ~~a~~ said shielding layer in said logic region.

9. (Amended) The semiconductor device according to claim 5, wherein ~~a potential of~~ said shielding layer ~~is~~ has a fixed potential.

10. (Amended) A method of fabricating a semiconductor device having at least ~~a~~ one DRAM region and ~~a~~ one logic region and having a resistor group in said logic region, the method comprising:

forming a resistor group in said logic region;

forming a shielding layer in said DRAM region and said logic region; and

forming a metal interconnection layer ~~above~~ opposite a portion of said logic region ~~in which~~ where said resistor group ~~has been formed~~ is located.

12. (Amended) The method according to claim 10, further comprising forming a stacked capacitor ~~composed of~~ having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said capacitor electrode layer is ~~used as~~ said shielding layer.

13. (Amended) The method according to claim 10, further comprising fixing ~~a~~ potential of said shielding layer.

14. (Amended) A method of fabricating a semiconductor device having at least ~~a~~

one DRAM region and ~~a~~ one logic region and having a signal interconnection layer in said logic region, the method comprising:

forming a signal interconnection layer in said logic region; and

forming a shielding layer on at least one side of said signal interconnection layer~~, or forming shielding layers on both sides of said signal interconnection layer,~~ in said DRAM region and said logic region.

17. (Amended) The method according to claim 14, further comprising forming a stacked capacitor ~~composed of~~ having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said capacitor electrode layer is ~~used as~~ said shielding layer.

18. (Amended) The method according to claim 14, further comprising fixing ~~a~~ potential of said shielding layer.

Amendments to the abstract:

ABSTRACT OF THE DISCLOSURE

A semiconductor device has a semiconductor substrate and a resistor group and/or a signal interconnection layer ~~on~~ in a region ~~in this~~ of the semiconductor substrate. A shielding layer ~~provided~~ is located above and/or below the region where the resistor group and/or the signal interconnection layer ~~has been provided~~ are located.

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For:	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME		

PENDING CLAIMS AFTER ENTRY OF PRELIMINARY AMENDMENT

1. A semiconductor device comprising:

a semiconductor substrate having a plurality of regions;

a resistor group including a plurality of resistors located in one of said regions of said semiconductor substrate;

a metal interconnection layer opposite the region in which said resistor group is located; and

a shielding layer between said resistor group and said metal interconnection layer.

2. The semiconductor device according to claim 1, comprising at least one DRAM region and one logic region, including a layer common to a bit line layer in said DRAM region and used as said shielding layer in said logic region.

3. The semiconductor device according to claim 1, comprising

at least one DRAM region with a stacked capacitor and one logic region, wherein said stacked capacitor in said DRAM region includes a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, and

a layer common to said upper capacitor electrode layer in said DRAM region and used as said shielding layer in said logic region.

4. The semiconductor device according to claim 1, wherein said shielding layer has a fixed potential.

5. A semiconductor device comprising:

a semiconductor substrate;

a signal interconnection layer on said semiconductor substrate; and

a shielding layer on at least one side of said signal interconnection layer.

6. The semiconductor device according to claim 5, comprising at least one DRAM region and one logic region, including a layer common to a gate electrode layer in said DRAM region and used as said shielding layer in said logic region.

7. The semiconductor device according to claim 5, comprising at least one DRAM region and one logic region, including a layer common to a bit line layer in said DRAM region and used as said shielding layer in said logic region.

8. The semiconductor device according to claim 5, comprising

at least one DRAM region with a stacked capacitor and one logic region, wherein said stacked capacitor in said DRAM region includes a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, and

a layer common to said upper capacitor electrode layer in said DRAM region and used as said shielding layer in said logic region.

9. The semiconductor device according to claim 5, wherein said shielding layer has a fixed potential.

10. A method of fabricating a semiconductor device having at least one DRAM region and one logic region and having a resistor group in said logic region, the method comprising:

forming a resistor group in said logic region;

forming a shielding layer in said DRAM region and said logic region; and

forming a metal interconnection layer opposite a portion of said logic region where said resistor group is located.

11. The method according to claim 10, wherein said shielding layer is a bit line layer.

12. The method according to claim 10, further comprising forming a stacked capacitor having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said capacitor electrode layer is said shielding layer.

13. The method according to claim 10, further comprising fixing potential of said shielding layer.

14. A method of fabricating a semiconductor device having at least one DRAM region and one logic region and having a signal interconnection layer in said logic region, the method comprising:

forming a signal interconnection layer in said logic region; and

forming a shielding layer on at least one side of said signal interconnection layer in said DRAM region and said logic region.

15. The method according to claim 14, wherein said shielding layer is a gate electrode layer.

16. The method according to claim 14, wherein said shielding layer is a bit line layer.

17. The method according to claim 14, further comprising forming a stacked capacitor having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said capacitor electrode layer is

said shielding layer.

18. The method according to claim 14, further comprising fixing potential of said shielding layer.

FIG.6A

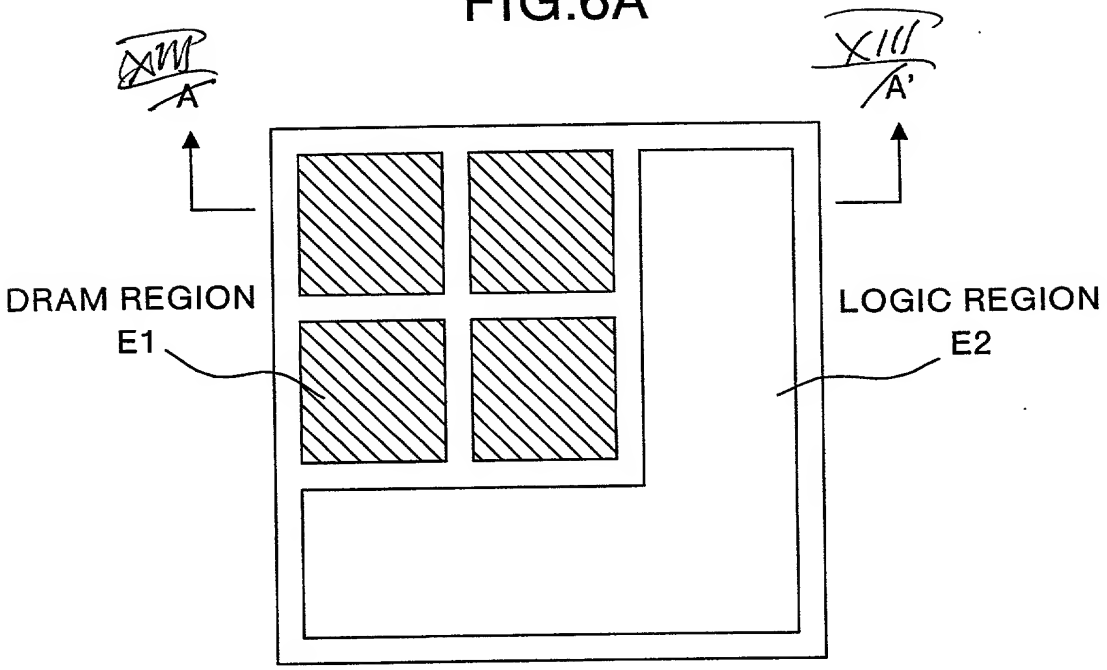
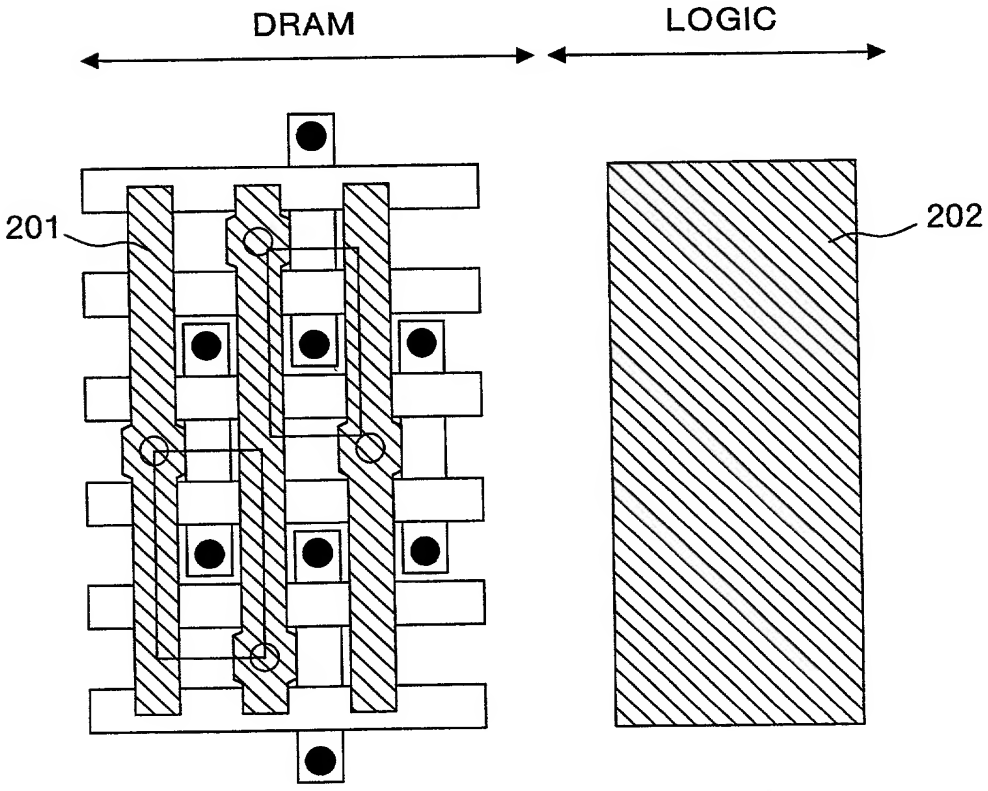

XIII
A
XIII
A'
DRAM REGION
E1
LOGIC REGION
E2

FIG.6B


DRAM
LOGIC
201
202